VLSI Introduction HWI

Inverter

Due Day: 10/30, 2017

Please do the simulation and analysis for CMOS inverter with CIC018.l.

The assignment should be done under the following condition.

1. The length of NMOS and PMOS should be 1X minimum channel length of this technology node.
2. The width of NMOS should be 1X and 5X minimum channel width of this technology node.
3. Power supply (VDD) = 1.8V
4. The output load of CMOS inverter is 0.1pF.
5. Please find the optimized PMOS size for balanced trigger point of inverter in five different Process corners and Temperature conditions. The meaning of balanced trigger point is as the following.

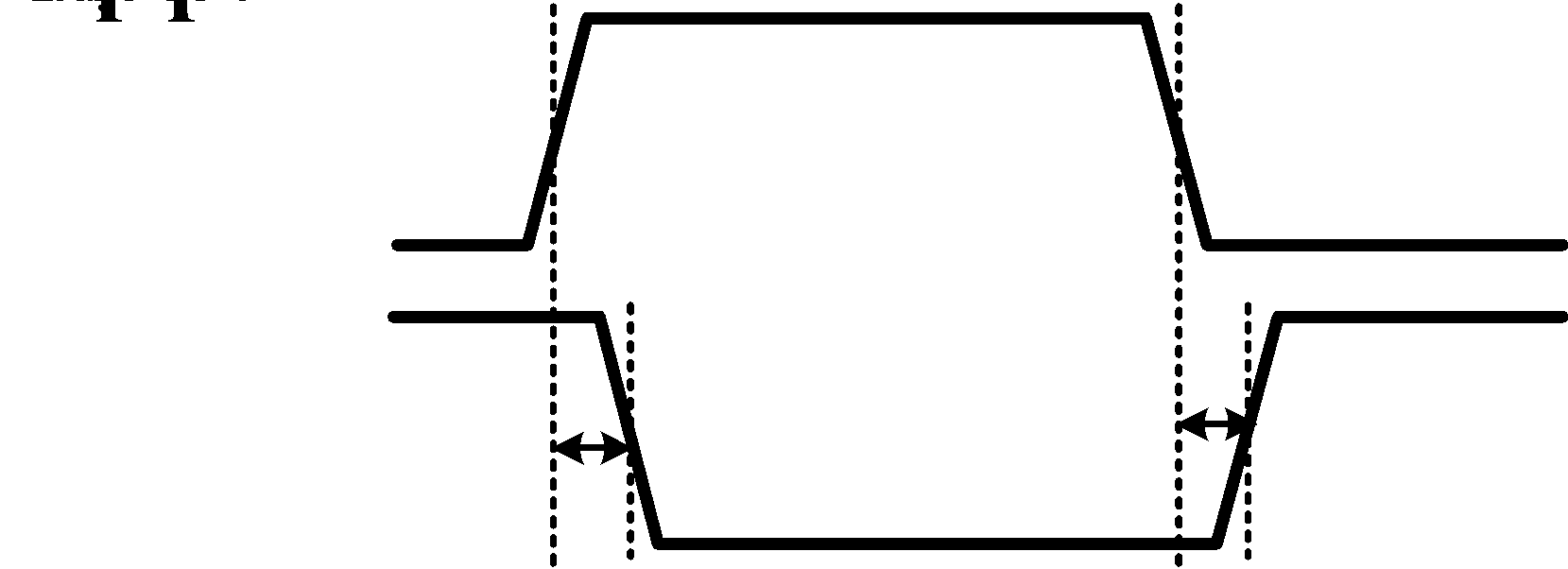
***Inverter Input = Inverter Output = 0.5VDD***

| Corner | Temperature | NMOS Width 1X | NMOS Width 5X |
| --- | --- | --- | --- |
| PMOS Width | PMOS Width |
| TT | 25 | 1.1um | 3.86um |
| FF | -40 | 1.24um | 4.09um |
| SS | 125 | 0.8um | 3.17um |
| SF | 25 | - | 1.11um |
| FS | 25 | 0.75um | 2.83um |

Note. The length of PMOS and NMOS should be equal to minimum length.

Please print out both Input and Output waveforms in each condition and mark with the transistor size on the report.

1. Followed by part A, please use the acquired size as conditions to observe the phenomenon of inverter output delay in three different conditions. The applied input pulse should be 1ns rise time and fall time.



| Corner | Temperature | NMOS Width 1X | NMOS Width 5X |
| --- | --- | --- | --- |
| TT | 25 | fall\_delay= 674.2710ps  rise\_delay= 532.7956ps | fall\_delay= 256.0430ps  rise\_delay= 263.0633ps |
| FF | -40 | fall\_delay= 518.3305ps  rise\_delay= 445.6919ps | fall\_delay= 202.7219ps  rise\_delay= 210.2150ps |
| SS | 125 | fall\_delay= 1.6729ns  rise\_delay= 1.2453ns | fall\_delay= 499.0276ps  rise\_delay= 485.8732ps |

Note: The report should add up your observations and comments.

No plagiarism is allowed.